What is claimed is:

1. An electromagnetic disturbance analysis method for analyzing an external noise to a semiconductor integrated circuit comprising:

an impedance extraction step of extracting impedance information on the power wiring in the target semiconductor integrated circuit or the power wiring in the semiconductor integrated circuit and the external power wiring of the semiconductor integrated circuit;

an equivalent circuit creating step of creating an equivalent circuit from said impedance information; and

an analysis step of supplying a noise waveform externally and analyzing the influence of the noise on said semiconductor integrated circuit.

2. The electromagnetic disturbance analysis method according to claim 1, wherein said analysis step includes:

a noise waveform supplying step of supplying a start point power noise waveform;

a power noise waveform calculating step of obtaining power noise waveforms at the internal node points and terminals in said semiconductor integrated circuit; and

an error section detecting step of obtaining the influence of an external noise on the semiconductor integrated circuit

and detecting sections susceptible to an external noise entering said semiconductor integrated circuit.

3. The electromagnetic disturbance analysis method according to claim 1,

wherein said equivalent circuit creating step comprises: a functional block power equivalent circuit creating step of creating a degenerate impedance circuit of each functional block in a semiconductor integrated circuit from said impedance information; and an inter-block power equivalent circuit creating step of creating a circuit for analyzing the inter-block power wiring in the semiconductor integrated circuit from said impedance information,

wherein said analysis step uses as said equivalent circuit at least one of said degenerate impedance circuit and said circuit for analyzing the inter-block power wiring.

4. The electromagnetic disturbance analysis method according to claim 1,

wherein said equivalent circuit creating step comprises: a functional block power equivalent circuit creating step of creating a degenerate impedance circuit of each functional block in a semiconductor integrated circuit from said impedance information; and an inter-block power equivalent circuit creating step of creating a circuit for analyzing the inter-block

power wiring in the semiconductor integrated circuit from said impedance information and an external power equivalent circuit creating step of creating an a circuit for analyzing the power wiring external to the semiconductor integrated circuit from said impedance information,

wherein said analysis step uses as said equivalent circuit at least one of said degenerate impedance circuit, said circuit for analyzing the inter-block power wiring and said circuit for analyzing the power wiring external to the semiconductor integrated circuit.

5. The electromagnetic disturbance analysis method according to claim 3,

wherein said inter-block power equivalent circuit creating step is a step of creating said circuit for analyzing the inter-block power wiring by adding the impedance information on said inter-block power wiring to said degenerate impedance circuit created by said functional block power equivalent circuit creating step,

wherein said analysis step uses as said equivalent circuit at least one of said degenerate impedance circuit and said circuit for analyzing the inter-block power wiring.

6. The electromagnetic disturbance analysis method according to claim 4,

wherein said inter-block power equivalent circuit creating step is a step of creating said circuit for analyzing the inter-block power wiring by adding the impedance information on said inter-block power wiring to said degenerate impedance circuit created by said functional block power equivalent circuit creating step,

wherein said external power equivalent circuit creating step is a step of configuring a circuit for analyzing the power wiring external to the semiconductor integrated circuit by creating a degenerate impedance circuit in said circuit for analyzing the inter-block power wiring and adding the impedance information external to the semiconductor integrated circuit to said degenerate impedance circuit,

wherein said analysis step uses as said equivalent circuit at least one of said degenerate impedance circuit, said circuit for analyzing the inter-block power wiring and said circuit for analyzing the power wiring external to the semiconductor integrated circuit.

7. The electromagnetic disturbance analysis method according to claim 2,

wherein said noise waveform supplying step is a step of supplying a start point power noise waveform to the power terminal in a circuit for analyzing the inter-block power wiring created from said impedance information,

wherein said power noise waveform calculating step comprises: an inter-block power noise calculating step of obtaining an inter-block power noise waveform at each internal node point in said circuit for analyzing the inter-block power wiring as well as obtaining a block terminal power noise waveform at a terminal in each functional block; and an intra-functional-block power noise waveform calculating step of obtaining a functional block power noise waveform at each node point in said functional block as well as obtaining an element terminal power noise waveform at the power terminal in each element by providing as input said block terminal power noise waveform to the impedance circuit in the functional block created from said impedance information,

wherein the circuit section expected to be susceptible to an external noise by using at least one of said block terminal power noise waveform, said inter-block power noise waveform, said functional block power noise waveform and said element terminal power noise waveform is identified.

8. The electromagnetic disturbance analysis method according to claim 2,

wherein said noise waveform supplying step is a step of supplying a start point power noise waveform to the power terminal in a circuit for analyzing the power wiring external to the semiconductor integrated circuit created from said

impedance information,

wherein said power noise waveform calculating step comprises: external power noise waveform calculating step of obtaining a terminal power noise waveform at the power terminal in a circuit for analyzing the inter-block power wiring created from said impedance information through said circuit for analyzing the power wiring external to the semiconductor integrated circuit; an inter-block power noise calculating step of obtaining an inter-block power noise waveform at each internal node point of said inter-block power wiring as well as obtaining a block terminal power noise waveform at a terminal in each functional block; and an intra-functional-block power noise waveform calculating step of obtaining a functional block power noise waveform at each node point in said functional block as well as obtaining an element terminal power noise waveform at the power terminal of each element by providing as input said block terminal power noise waveform to the impedance circuit in the functional block

wherein the circuit section expected to be susceptible to an external noise by using at least one of said terminal power noise waveform, said block terminal power noise waveform, said inter-block power noise waveform, said functional block power noise waveform and said element terminal power noise waveform is identified.

9. The electromagnetic disturbance analysis method according to claim 2, wherein said error section detecting step comprises an error check step of identifying the circuit sections that will cause an error due to an external noise by providing a power noise peak threshold for said power noise waveform and assuming an error when said threshold is exceeded thus performing an error check.

10. The electromagnetic disturbance analysis method according to claim 8, wherein said error section detecting step performs a noise check step of performing a noise check by providing a threshold at the power terminal in said circuit for analyzing the inter-block power wiring and assuming an error when said threshold is exceeded and performs said inter-block power noise waveform calculating step only when an error is determined.

11. The electromagnetic disturbance analysis method according to claim 10, wherein the threshold at the power terminal in the circuit for analyzing the inter-block power wiring is the maximum among the thresholds for the terminal in the functional block in said semiconductor integrated circuit and inter-block power wiring.

12. The electromagnetic disturbance analysis method

according to claim 7, wherein said error section detecting step performs a noise check step of performing a noise check by providing a peak threshold for a power noise at each functional block in a semiconductor integrated circuit and assuming an error when said threshold is exceeded at the power terminal in said functional block and performs said intra-functional-block power noise waveform calculating step only when an error is determined.

13. The electromagnetic disturbance analysis method according to claim 12, wherein the threshold for a power noise at the power terminal in each functional block is the maximum of the thresholds for the functional elements in each functional block and power wiring.

14. The electromagnetic disturbance analysis method according to claim 9, wherein said error check step comprises a noise check step of performing a noise check by providing a peak threshold for a power noise at each functional element in a semiconductor integrated circuit and assuming an error when the power noise peak value has exceeded said threshold.

15. The electromagnetic disturbance analysis method according to claim 9, wherein said error check step comprises a noise check step of performing a noise check by providing

a peak threshold for a power noise determined by the distance to an adjacent signal line and length of parallel wiring for the power wiring in each functional block or inter-block power wiring and assuming an error when the power noise peak value has exceeded said threshold at each internal node points of said power wiring.

16. An Electromagnetic disturbance analysis apparatus comprising:

extraction unit for extracting impedance information on the power wiring in the target semiconductor integrated circuit or the power wiring in the semiconductor integrated circuit and the external power wiring of the semiconductor integrated circuit;

equivalent circuit creating unit for creating an equivalent circuit from said impedance information; and

analysis unit for supplying a noise waveform externally and analyzing the influence of the noise on said semiconductor integrated circuit.

17. The electromagnetic disturbance analysis method according to claim 1, wherein said analysis step comprises:

a step of obtaining a power waveform at the power terminal of each circuit element in said semiconductor integrated circuit;

a calculating step of calculating the delay time of said circuit element based on the power waveform at the power terminal of said circuit element; and

a timing verification step of determining whether the delay time of said circuit element is within an allowable range.

18. The electromagnetic disturbance analysis method according to claim 1, wherein said analysis step comprises:

a step of obtaining a power waveform at the power terminal of each circuit element in said semiconductor integrated circuit;

a calculating step of calculating the delay time of said circuit element based on the power waveform at the power terminal of said circuit element; and

a timing verification step of determining whether the sum of the delay times of said series of circuit elements is within an allowable range.

19. The electromagnetic disturbance analysis method according to claim 17,

wherein said analysis step further comprises a database creating step of calculating the variation amount in the delay time of a circuit element obtained when at least one of the input timing and peak value of the noise waveform of said power terminal is varied and creating a delay variation amount database

based on the calculation result,

wherein said calculating step comprises a step of obtaining the variation amount of the delay time of said circuit element with respect to a desired noise waveform from said delay variation amount database.

20. The electromagnetic disturbance analysis method according to claim 17, wherein said analysis step further comprises a database creating step of calculating the variation amount in the delay time of a circuit element obtained when at least one of the input timing and peak value of the noise waveform of said power terminal is varied and creating a delay variation rate database by obtaining the calculation result as a rate to the delay time of the circuit element observed when no power noises are present,

wherein said calculating step comprises a step of obtaining the delay variation amount of the circuit element with respect to a desired noise, by multiplying the delay time of the circuit element observed when no power noises are present by said rate read from said delay variation rate database.

21. The electromagnetic disturbance analysis method according to claim 18,

wherein said analysis step comprises a step of obtaining the delay variation amount of said series of circuit elements

with the timing the power noise where the variation amount of each circuit element is the maximum is input to said series of circuit element, as the maximum delay amount of said series of circuit elements.

22. The electromagnetic disturbance analysis method according to claim 1, wherein said analysis step comprises a step of detecting a circuit section where a signal does not arrive within a time required for circuit operation due to a variation in the delay time of a circuit element caused by a power noise thus resulting in an unexpected circuit operation.

23. The electromagnetic disturbance analysis method according to claim 22 further comprises an error element detecting step of exploring a circuit element whose delay time is most affected by a power noise from said detected circuit section and detecting the circuit element as an error element.

24. The electromagnetic disturbance analysis method according to claim 23 further comprises a reinforcing step of taking power noise hardening countermeasures on said error element.

25. The electromagnetic disturbance analysis method according to claim 23 further comprises a replacing step of

replacing the circuit element assumed as an error element in said error element detecting step with a circuit element whose delay variation amount with respect to a power noise is smaller.

26. The electromagnetic disturbance analysis method according to claim 23 further comprises a replacing step of replacing the circuit element assumed as an error element in said error element detecting step with a circuit element which satisfies a constraint time.

27. The semiconductor device manufacturing method comprises a step of manufacturing a semiconductor device through error-free layout design based on the analysis result using an electromagnetic disturbance analysis method according to claims 1.

28. An electromagnetic disturbance analysis method for analyzing an electromagnetic disturbance in an LSI circuit comprising:

a library storage step of calculating a noise threshold for changing the output result or internal state caused by a power noise and storing the noise threshold into a library; and

an analysis step of analyzing whether each of the circuit elements in said LSI circuit suffer from the influence of the

power noise while referring to said library.

29. The electromagnetic disturbance analysis method according to claim 28, wherein said library storage step comprises a step of storing into a library any of the peak, width and shape functions or values of the voltage or current waveform that can pass through a circuit element.

30. The electromagnetic disturbance analysis method according to claim 28, wherein said library storage step comprises a step of storing into said library a noise threshold for a path on which a noise is input to the terminal of a circuit element and is output from the terminal of the circuit element or a path for changing the internal state.

31. The electromagnetic disturbance analysis method according to claim 28, wherein said analysis step comprises a step of analyzing a path on which a noise is input to the terminal of a circuit element and is output from the terminal of the circuit element or a path for changing the internal state.

32. The electromagnetic disturbance analysis method according to claim 28, wherein said analysis step comprises a recording step of recording path information.

33. The electromagnetic disturbance analysis method according to claim 32, wherein said recording step comprises a step of recording a circuit element where a noise is propagated.

34. The electromagnetic disturbance analysis method according to claim 32, wherein said recording step comprises a step of recording a register element where a noise is propagated.

35. The electromagnetic disturbance analysis method according to claim 32, wherein said recording step comprises a step of recording a damage when a circuit element where a noise is propagated is virtually changed to a circuit element with different drive capability.

36. The electromagnetic disturbance analysis method according to claim 32, wherein said recording step comprises a step of recording a circuit element susceptible to a noise on the path.

37. The electromagnetic disturbance analysis method according to claim 28, wherein said analysis step comprises a step of calculating said power noise analyzing electromagnetic wave.

38. The electromagnetic disturbance analysis method according to claim 28, wherein said analysis step comprises a step of recording a circuit element susceptible to a noise on the path entering a specified circuit element.

39. The electromagnetic disturbance analysis method according to claim 28, wherein said analysis step comprises a step of recording a circuit element susceptible to a noise on the path entering a register element.

40. An electromagnetic disturbance analysis apparatus for analyzing an electromagnetic disturbance in an LSI circuit comprising:

a library for storing the noise threshold for changing the output result or internal state depending on a power noise and storing the noise threshold into a library; and

an analysis unit which analyses whether each of the circuit elements in said LSI circuit suffer from the influence of the power noise while referring to said library.

41. An electromagnetic disturbance analysis method comprising:

a step of analyzing an electromagnetic disturbance in an LSI circuit;

a sorting step of sorting blocks or instances that need

countermeasures; and

a countermeasure step of taking countermeasures to erase a power noise on each block or instance.

42. The electromagnetic disturbance analysis method according to claim 41, further comprising a step of analyzing EMS of the block or instance after said countermeasure step,

wherein said countermeasure step and analysis step are repeated until the influence of the power noise is found below a predetermined value in said analysis step.

43. The electromagnetic disturbance analysis method according to claim 42, wherein said countermeasure step is a step of inserting a delay adjustment element for performing delay adjustment so that a switching element will become highly resistant with the timing a current including a noise enters the switching element and an RC filter circuit formed by said switching element and a capacitance element.

44. The electromagnetic disturbance analysis method according to claim 42, wherein said countermeasure step is a step of inserting an inductor.

45. The electromagnetic disturbance analysis method according to claim 42, wherein said countermeasure step is a

step of adjusting the power wiring length distance.

46. The electromagnetic disturbance analysis method according to claim 42, wherein said countermeasure step is a step of changing the cell rank so that the drive capability of the cell with sufficient timing will be reduced.

47. An electromagnetic disturbance countermeasure apparatus comprising:

unit for analyzing an electromagnetic disturbance in an LSI circuit;

sorting unit for sorting blocks or instances that need countermeasures; and

countermeasure unit for taking countermeasures to erase a power noise on each block or instance in accordance with the order arranged by said sorting unit.

48. The electromagnetic disturbance countermeasure apparatus according to claim 47 further comprising unit for analyzing EMS of the block or instance that undertook countermeasures in said countermeasure unit,

wherein said countermeasure step and analysis step are repeated until the influence of the power noise is found below a predetermined value in said analysis step.

49. The electromagnetic disturbance analysis method according to claims 1 further comprising a display step of highlighting cells susceptible to a noise and paths connecting the cells as analyzed in said analysis step.

50. The electromagnetic disturbance analysis method according to claim 1 further comprising a display step of highlighting register cells such as memory cells.

51. The electromagnetic disturbance analysis method according to claim 1 further comprising a display step of displaying information on cells having been found susceptible to a noise and should be replaced in said analysis step.

52. The electromagnetic disturbance analysis method according to claim 1 further comprising a virtual display step of displaying parameters renewed for each cell virtually changed based on the information on cells that were analyzed to be replaced with spare in said analysis step.

53. The electromagnetic disturbance analysis method according to claim 1 further comprises a sorting step of sorting blocks or instances determined requiring countermeasures in said analysis step.

54. The electromagnetic disturbance analysis method according to claim 41 further comprising a countermeasure sorting step of sorting countermeasures to take on blocks or instances determined to require countermeasures in said analysis step.

55. The electromagnetic disturbance analysis method according to claim 8, wherein said error section detecting step performs a noise check step of performing a noise check by providing a peak threshold for a power noise at each functional block in a semiconductor integrated circuit and assuming an error when said threshold is exceeded at the power terminal in said functional block and performs said intra-functional-block power noise waveform calculating step only when an error is determined.

56. The electromagnetic disturbance analysis method according to claim 55, wherein the threshold for a power noise at the power terminal in each functional block is the maximum of the thresholds for the functional elements in each functional block and power wiring.

57. The electromagnetic disturbance analysis method according to claim 18,

wherein said analysis step further comprises a database

creating step of calculating the variation amount in the delay time of a circuit element obtained when at least one of the input timing and peak value of the noise waveform of said power terminal is varied and creating a delay variation amount database based on the calculation result,

wherein said calculating step comprises a step of obtaining the variation amount of the delay time of said circuit element with respect to a desired noise waveform from said delay variation amount database.

58. The electromagnetic disturbance analysis method according to claim 18, wherein said analysis step further comprises a database creating step of calculating the variation amount in the delay time of a circuit element obtained when at least one of the input timing and peak value of the noise waveform of said power terminal is varied and creating a delay variation rate database by obtaining the calculation result as a rate to the delay time of the circuit element observed when no power noises are present,

wherein said calculating step comprises a step of obtaining the delay variation amount of the circuit element with respect to a desired noise, by multiplying the delay time of the circuit element observed when no power noises are present by said rate read from said delay variation rate database.